Dual Input AND Gate Fabricated Using a Single Channel $\alpha$–sexithiophene Thin Film Field Effect Transistor

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Abstract

We have used a split gate field effect transistor configuration to construct a dual input logic AND gate. The device in this configuration consists of a source, a drain and two gate terminals that are positioned between the source and the drain terminals and which lie under the insulating dielectric layer. The active semiconductor used in this device was $\alpha$-sexithiophene. This is a commercially available organic semiconducting molecule and can be evaporated to form uniform thin films under reduced pressure. The transistor operation was controlled by applying either 0 or -10 V to each gate electrode. When -10 volts was simultaneously applied to both gates the device was conductive. Any other combination of gate voltages rendered the device resistive. This shows that the device operates like a logic AND gate. The electric field charge mobility in this device was calculated to be $\approx 10^{-4}$ cm²/V.s and is partially attributed to the substrate topography which is not planar. The device ON/OFF ratio was ~5. These device parameters are expected to improve via the use of purified starting materials, pretreated substrates and a more planar channel topography. A significant advantage of this configuration is that AND logic devices with multiple inputs can be fabricated using a single $\alpha$-sexithiophene channel with multiple gates and which in turn will lead to the fabrication of more compact electronic circuitry at reduced cost.

Keywords: organic, semiconductor, device

1. Introduction

$\alpha$-Sexithiophene is one of the widely studied organic semiconducting molecules that has a high mobility and ON/OFF ratio when configured to work in a field effect transistor (FET) configuration, two important device parameters that make it viable for use in practical circuits. Technologically, the most important polymer based device fabricated and studied is the FET since it forms the basic building block in logic circuits and switches for displays. In this paper, a modified FET architecture has been designed that uses a split gate configuration as shown in the schematic diagram in Figure 1 so that each gate can be independently addressed. Our previous results on the use of such a design in the case of pentacene have now been extended to $\alpha$-sexithiophene. We show that a thermally evaporated thin film of $\alpha$-sexithiophene single channel split-gate FET functions as a dual input logic AND gate. Since numerous logic circuits that require multiple inputs are widely used in devices such as comparators, the fact that this functionality can be achieved using a single transistor, rather than cascading a series of single input transistors, could reduce the number of transistors required in many digital applications thereby making the device
more compact. We correlate the measured electrical performance of this device with film morphology and substrate
design.

![Figure 1. Schematic of a split gate field effect transistor.](image)

2. Experimental Procedure

A view of the split-gate field effect transistor structure is schematically illustrated in Figure 1. The semiconductor
that was used to prepare the device was $\alpha$-sexithiophene. This semiconductor was purchased from Aldrich
chemicals and used as received. Figure 2 below shows the chemical structure of
$\alpha$-sexithiophene which is a $\pi$ conjugated molecule.

![Figure 2. Chemical structure of $\alpha$-sexithiophene](image)

A thin film of $\alpha$-sexithiophene was deposited over the substrate in a thermal evaporator. The device was fabricated
as follows: The starting wafer is n-type doped Si (10 $\Omega$ cm), with a 200 nm thick thermally grown oxide layer. First,
the gate metals comprise of 20 nm Cr/100 nm Au, were vacuum deposited in a thermal evaporator and patterned
using conventional photolithographic and liftoff techniques. Next, a 100 nm thick silicon dioxide film, SiO$_2$ (gate
dielectric) was deposited over this using chemical vapor deposition. Figure 3(a) shows the top view of the substrate
prior to the deposition of $\alpha$-sexithiophene and Figure 3(b) shows the top view of the same substrate after the
deposition of $\alpha$-sexithiophene. Electrical contacts of the various electrodes were made via the used of gold wire and
silver paint.

![Figure 3. Optical images of the device substrate before (a) and after (b) the $\alpha$-sexithiophene deposition.](image)

The electrical current versus voltage characteristics of the devices were measured using a Keithley model 6517A
Electrometer under a vacuum pressure of $4 \times 10^{-4}$ torr. Gate voltages were applied with a Keithley model 6487
picoammeter/voltage source. Measurements were taken with the source electrode grounded, hence the gate 1, gate 2
and drain voltages are referenced to the source.
3. Results and Discussion

The drain-source current ($I_{DS}$) versus drain-source voltage ($V_{DS}$) characteristics of the split-gate transistor are shown in Figure 4 for various combinations of gate voltages $V_{GS1}$ and $V_{GS2}$ which correspond to the voltage applied to the two buried gate electrodes lying in between the drain and source electrodes respectively as seen in Figures 3. For each scan, the bias on the gate electrodes was either 0 or -10 volts, thus permitting four possible combinations of gate voltages. At a drain-source bias of -20V the current is significantly higher when both gate electrodes are biased with -10V. For the other combinations there was a smaller current primarily due to the low intrinsic conductivity of $\alpha$-sexithiophene and perhaps due to the unintentional doping of the semiconductor in air. Similar results are also seen for other values of common gate bias voltages viz. $I_{DS}$ was higher only when both gates were biased high simultaneously. Thus this device has characteristics similar to a dual input logic AND gate. As a simple model, our results can be explained by treating the device as consisting of two gate voltage controlled switches connected in series and which lead to the logical AND operation via ON/OFF operation of these switches. Due to the uneven substrate topography, especially at the step edges of the gate electrodes as seen via the AFM, the charge mobility in this device is expected to be adversely affected which in turn will lead to inferior device characteristics. From Figure 4 we can estimate this value from the linear portion of the curves corresponding to the common gate voltages of 0V and -10V. The device transconductance ($g_m$) is given by equation (1).

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} \bigg|_{V_{DS}=\text{const}}$$

Treating the transistor as a single gate structure, with $V_{GS1} = V_{GS2} = -10$ V and $V_{DS} = -1.0$ V, $g_m$ is calculated to be $1.07 \times 10^{-11}$ S. The carrier mobility is then determined using equation (2).

$$\mu = \frac{g_m L}{Z C_i V_D}$$

where L is the channel length (52 µm), Z is the channel width (600 µm), and $C_i$ is the capacitance per unit area of the 100 nm thick silicon dioxide layer ($17.5 \times 10^{-5}$ F/cm²). In the linear region, the mobility is calculated to be $2.2 \times 10^{-4}$ cm²/V-sec.

![Figure 4](image_url)

Figure 4. a) Drain-source current versus drain-source voltage ($I_{DS}$-$V_{DS}$) characteristics of the split gate field effect transistor, where the gate-source voltages ($V_{GS1}$ and $V_{GS2}$) are as indicated. b) The equivalent dual input AND gate with the truth table.

In order to further characterize the device, a series of measurements having both gates biased with a common voltage has been done. Figure 5 shows the characteristic curves of this experiment. At low drain
source voltages the channel current is linear but at voltages comparable to and larger than the gate-source bias, the drain-source current begins to near saturation. The increase in the drain-source current for fixed \( V_{DS} \) upon increasing the negative gate bias demonstrates that the device operates as a FET.

![Figure 5. Drain source current versus drain-source voltage (\( I_{DS}-V_{DS} \)) characteristics of the split gate field effect transistor, where the gate-source voltages (\( V_{GS1}=V_{GS2} \)) are as indicated.](image)

4. Conclusions

A split-gate field effect transistor with a thin film of \( \alpha \)-sexithiophene as the active semiconducting layer was fabricated and characterized. This device was seen to work as a dual input logic AND gate and was operated by applying 0 or -10 volts to each of the gate electrodes. When -10 volts was simultaneously applied to both gates, the transistor was conductive, while any other combination of gate voltages rendered the transistor resistive. The device also worked as a field effect transistor with a dynamic ratio of ~ 5 and had a charge carrier mobility of ~ \( 10^{-4} \) cm²/V.s. These device parameters are expected to improve via the use of purified starting materials, pretreated substrates and more planar channel topography. A significant advantage of this device is that AND logic devices with multiple inputs can be built using a single \( \alpha \)-sexithiophene channel with multiple gates.

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6. References